National Semiconductor

May 2004

# LM41
# Hardware Monitor with Thermal Diode Inputs and SensorPath™ Bus

## General Description

The LM41 is a hardware monitor that measures 2 temperature zones, 5 voltages and has a single-wire interface compatible with National Semiconductor's SensorPath bus. SensorPath data is pulse width encoded, thereby allowing the LM41 to be easily connected to many general purpose micro-controllers. Several National Semiconductor Super I/O products include a fully integrated SensorPath master, that when connected to the LM41 can realize a hardware monitor function that includes limit checking for measured values, autonomous fan speed control and many other functions.

The LM41 measures the temperature of its own die as well as one external device such as a processor thermal diode or a diode connected transistor. The LM41 can resolve temperatures up to 255˚C and down to -256˚C. The operating temperature range of the LM41 is 0˚C to +125˚C. Using ΣΔ ADC it measures +1.2V, +2.5V, +3.3V, +5V and +12V analog input voltages with internal scaling resistors. The address programming pin allows two LM41's to be placed on one SensorPath bus.

## Features

- SensorPath Interface
  - — 2 hardware programmable addresses
- Voltage Monitoring
  - — 9-bit ΣΔ ADC
  - — Internal scaling resistors for all inputs
  - — Monitors +1.2V, +2.5 V, +3.3 V, +5 V and +12 V
- Temperature Sensing
  - — Remote diode temperature sensor zone
  - — Internal local temperature zone
  - — 0.5 ˚C resolution
  - — Measures temperatures up to 140 ˚C
- 14-lead TSSOP package

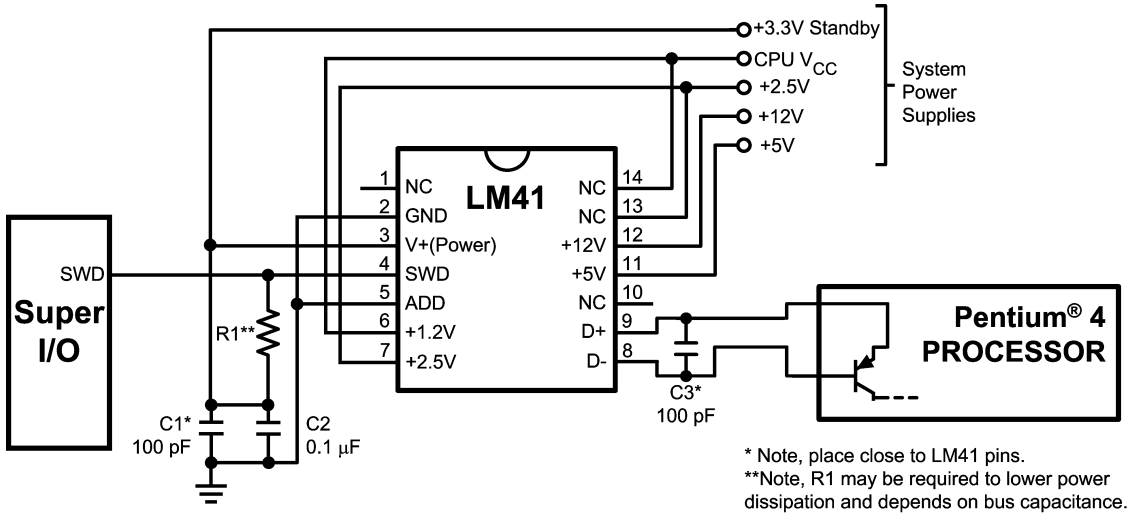
## Key Specifications

| | |
|---|---|
| ■ Voltage Measurement Accuracy | ±2 % (max) |
| ■ Temperature Sensor Accuracy | ±3 ˚C (max) |
| ■ Temperature Range: | |
| — LM41 junction | 0 ˚C to +85 ˚C |
| — Remote Temp Accuracy | 0 ˚C to +100 ˚C |
| ■ Power Supply Voltage | +3.0 V to +3.6 V |
| ■ Average Power Supply Current | 0.5 mA (typ) |
| ■ Conversion Time (all Channels) | 22.1ms to 1456ms |

## Applications

- Microprocessor based equipment
  (Motherboards, Video Cards, Base-stations, Routers, ATMs, Point of Sale, …)
- Power Supplies

## Typical Application




* Note, place close to LM41 pins.
**Note, R1 may be required to lower power dissipation and depends on bus capacitance.

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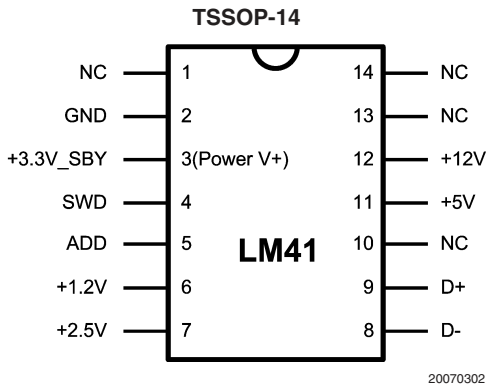
## Connection Diagram



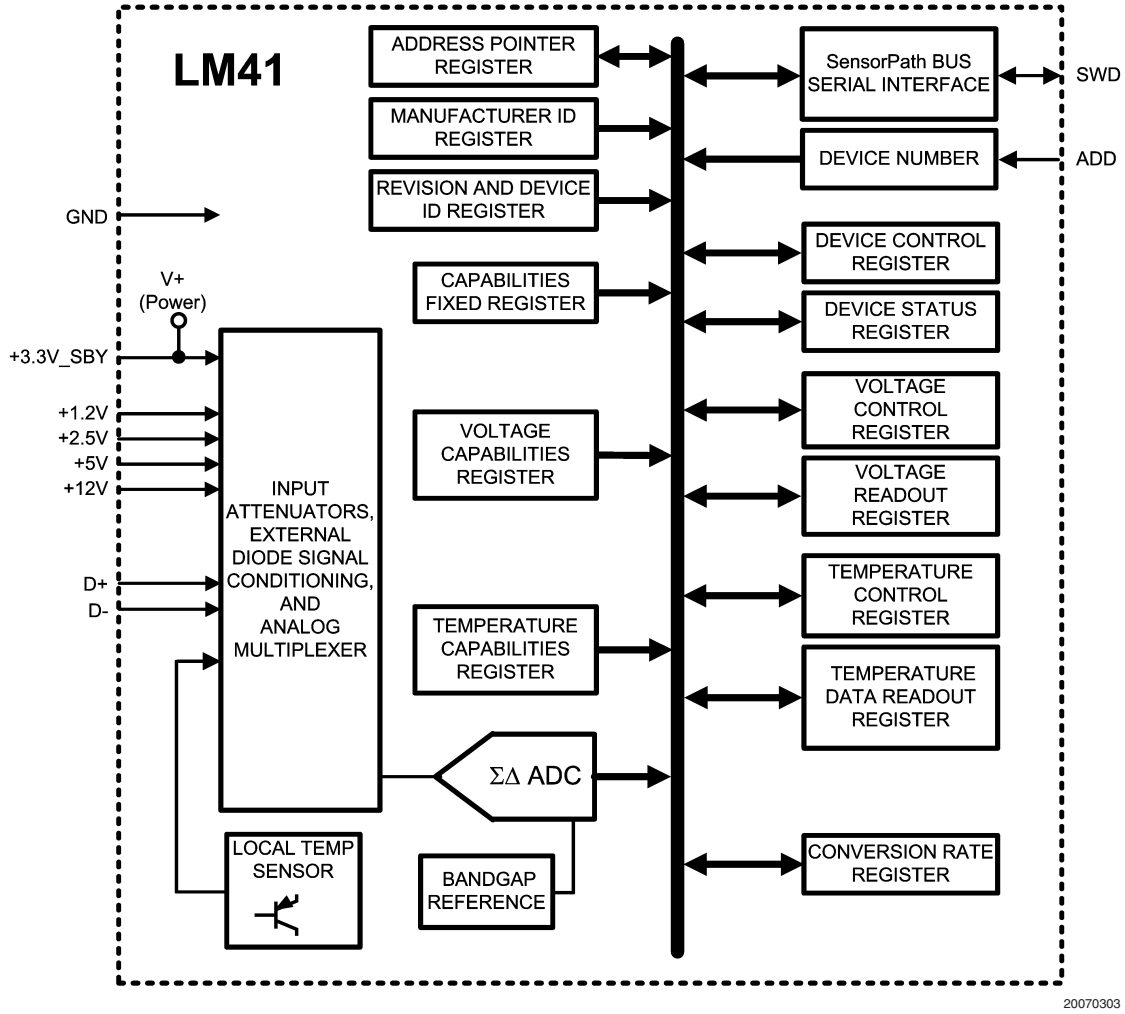

**Top View**
**National Package Number MTC14C**

| Order Number | Package Marking | NS Package Number | Transport Media |
|---|---|---|---|
| LM41CIMT | LM41 CIMT | MTC14C | 94 units per rail |
| LM41CIMTX | LM41 CIMT | MTC14C | 2500 units in tape and reel |

## Pin Description

| Pin Number | Pin Name | Description | Typical Connection |
|---|---|---|---|
| 1, 10, 13, 14 | NC | No Connect | May be tied to V+, GND or left floating. Do not tie active signals to pin 10. |
| 2 | GND | Ground | System ground |
| 3 | V+/+3.3V_SBY | Positive power supply pin as well as a +3.3V voltage monitor | Connected system 3.3 V standby power and to a 0.1 µF bypass capacitor in parallel with 100 pF. A bulk capacitance of approximately 10 µF needs to be in the near vicinity of the LM41. |
| 4 | SWD | SensorPath Bus line; Open-drain output | Super I/O, Pull-up resistor, 1.6k |
| 5 | ADD | Digital input - device number select input for the serial bus device number | Pull-up to 3.3 V or pull-down to GND resistor, 10k; must never be left floating |
| 6 | +1.2V | +1.2V voltage monitoring input with scaling resistors | Processor core voltage to be monitored |
| 7 | +2.5V | +2.5V voltage monitoring input with scaling resistors | Power supply voltage to be monitored |
| 8 | D- | Thermal diode analog voltage output and negative monitoring input | Remote Thermal Diode cathode (THERM_DC) - Can be connected to a CPU or thermal diode, an MMBT3904 or a GPU thermal diode. A 100 pF capacitor should be connected between respective D- and D+ for noise filtering. |
| 9 | D+ | Thermal diode analog current output and positive monitoring input | Remote Thermal Diode anode (THERM_DA) - Can be connected to a CPU or thermal diode, an MMBT3904 or a GPU thermal diode. A 100 pF capacitor should be connected between respective D- and D+ for noise filtering. |
| 11 | +5V | +5V voltage monitoring input with scaling resistors | Power supply voltage to be monitored |
| 12 | +12V | +12V voltage monitoring input with scaling resistors | Power supply voltage to be monitored |

## Block Diagram

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## Absolute Maximum Ratings

(Notes 2, 1)

| | |
|---|---|
| Supply Voltage ($V^+$) | −0.5 V to 6.0 V |
| Voltage at Any Digital Input or Output Pin | −0.5 V to 6.0 V |
| Voltage on 12V Analog Input | −0.5 V to 16 V |
| Voltage on 5V Analog Input | −0.5 V to 6.67 V |
| Voltage on D+ | −0.5 V to (V+ + 0.05 V) |
| Voltage on Other Analog Inputs | −0.5 V to 6.0 V |
| Current on D- | ±1 mA |
| Input Current per Pin(Note 3) | ±5 mA |
| Package Input Current (Note 3) | ±30 mA |
| Package Power Dissipation | (Note 4) |
| Output Sink Current | 10 mA |
| ESD Susceptibility (Note 5) | |
| Human Body Model | 2500 V |
| Machine Model | 250 V |
| Storage Temperature | −65˚C to +150˚C |

*Soldering process must comply with National's reflow temperature profile specifications. Refer to www.national.com/packaging/.* (Note 6)

## Operating Ratings

(Notes 1, 2)

| | |
|---|---|
| Temperature Range for Electrical Characteristics | |
| LM41CIMT ($T_{MIN} \le T_A \le T_{MAX}$) | $0˚C \le T_A \le +85˚C$ |
| Operating Temperature Range | $0˚C \le T_A \le +125˚C$ |
| Remote Diode Temperature ($T_D$) Range | $-5˚C \le T_D \le +140˚C$ |
| Supply Voltage Range (V+) | +3.0 V to +3.6 V |
| Analog Input Voltage Rage: | |
| +1.2V and +2.5V | −0.05V to (V+ + 0.05V) |
| +3.3V_SBY (V+) | +3.0V to +3.6V |
| +5V | −0.05V to +6.67V |
| +12V | −0.05V to +16V |

## DC Electrical Characteristics

The following specifications apply for V+ = +3.0 $V_{DC}$ to +3.6 $V_{DC}$, and all analog source impedance $R_S$ = 50 Ω unless otherwise specified in the conditions. **Boldface limits apply for LM41CIMT $T_A = T_J = T_{MIN}$=0˚C to $T_{MAX}$=85˚C;** all other limits $T_A$ = +25˚C. $T_A$ is the ambient temperature of the LM41; $T_J$ is the junction temperature of the LM41; $T_D$ is the junction temperature of the remote thermal diode.

**POWER SUPPLY CHARACTERISTICS**

| Symbol | Parameter | Conditions | Typical (Note 7) | Limits (Note 8) | Units (Limit) |
|---|---|---|---|---|---|
| V+ | Power Supply Voltage | | 3.3 | **3.0**<br>**3.6** | V (min)<br>V (max) |
| $I+_{Shutdown}$ | Shutdown Power Supply Current | SensorPath Bus Inactive (Note 9) | 260 | **420** | µA (max) |
| $I+_{Average}$ | Average Power Supply Current | SensorPath Bus Inactive; all sensors enabled; $t_{CONV}$=182 ms; (Note 9) | | **900** | µA (max) |
| $I+_{Peak}$ | Peak Power Supply Current | SensorPath Bus Inactive (Note 9) | | **3.3** | mA (max) |
| | Power-On Reset Threshold Voltage | | | **1.6** | V (min) |
| | | | | **2.8** | V (max) |

**TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS**

| Parameter | Conditions | | Typical (Note 7) | Limits (Note 8) | Units (Limits) |
|---|---|---|---|---|---|
| Temperature Accuracy Using the Remote Thermal Diode, see (Note 12) for Thermal Diode Processor Type. | $T_J$ = 0˚C to +85˚C | $T_D$ = +25˚C | ±1 | ±2.5 | ˚C (max) |
| | $T_J$ = 0˚C to +85˚C | $T_D$ = 0˚C to +100˚C | | **±3** | ˚C (max) |
| | $T_J$ = 0˚C to +85˚C | $T_D$ = +100˚C to +125˚C | | **±4** | ˚C (max) |
| Temperature Accuracy Using the Local Diode | $T_J$ = 0˚C to +85˚C (Note 10) | | ±1 | **±3** | ˚C (max) |
| Remote Diode and Local Temperature Resolution | | | 10 | | Bits |
| | | | 0.5 | | ˚C |
| D− Source Voltage | | | 0.7 | | V |

**TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS**

| Parameter | Conditions | Typical (Note 7) | Limits (Note 8) | Units (Limits) |
|---|---|---|---|---|
| Diode Source Current | $(V_{D+} - V_{D-})$ = +0.65 V; High Current | 188 | 280 | µA (max) |
| | Low Current | 11.75 | | µA |
| Diode Source Current High Current to Low Current Ratio | | 16 | | |

**ANALOG TO DIGITAL CONVERTER CHARACTERISTICS**

| Symbol | Parameter | Conditions | Typical (Note 7) | Limits (Note 8) | Units (Limit) |
|---|---|---|---|---|---|
| TUE | Total Unadjusted Error(Note 11) | | | **±2** | %FS (max) |
| | Resolution | | | 9 | Bits |
| DNL | Differential Non-linearity | | 1 | | LSB |
| | Power Supply Sensitivity | | ±1 | | %/V |
| | Input Resistance, all analog inputs (total resistance of divider chain) | | 210 | **140** | kΩ (min) |
| | | | | **400** | kΩ (max) |

**SWD and ADD DIGITAL INPUT CHARACTERISTICS**

| Symbol | Parameter | Conditions | Typical (Note 7) | Limits (Note 8) | Units (Limit) |
|---|---|---|---|---|---|
| $V_{IH}$ | SWD Logical High Input Voltage | | | **2.1** | V (min) |
| | | | | **V+ + 0.5** | V (max) |
| $V_{IL}$ | SWD Logical Low Input Voltage | | | **0.8** | V (max) |
| | | | | **-0.5** | V (min) |
| $V_{IH}$ | ADD Logical High Input Voltage | | | **90% x V+** | V (min) |
| $V_{IL}$ | ADD Logical Low Input Voltage | | | **10% x V+** | V (max) |
| $V_{HYST}$ | Input Hysteresis | | 300 | | mV |
| $I_L$ | SWD and ADD Input Current | $GND \le V_{IN} \le V+$ | ±0.005 | **±10** | µA (max) |
| | SWD Input Current with V+ Open or Grounded | $GND \le V_{IN} \le 3.6V$, and V+ Open or GND | ±0.005 | | µA |
| $C_{IN}$ | Digital Input Capacitance | | 10 | | pF |

**SWD DIGITAL OUTPUT CHARACTERISTICS**

| Symbol | Parameter | Conditions | Typical (Note 7) | Limits (Note 8) | Units (Limit) |
|---|---|---|---|---|---|
| $V_{OL}$ | Open-drain Output Logic "Low" Voltage | $I_{OL}$ = 4mA | | **0.4** | V (max) |
| | | $I_{OL}$ = 50µA | | **0.2** | V (max) |
| $I_{OH}$ | Open-drain Output Off Current | | ±0.005 | **±10** | µA (max) |
| $C_{OUT}$ | Digital Output Capacitance | | 10 | | pF |

## AC Electrical Characteristics

The following specification apply for V+ = +3.0 $V_{DC}$ to +3.6 $V_{DC}$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$=0˚C to $T_{MAX}$=85˚C**; all other limits $T_A = T_J$ = 25˚C. The SensorPath Characteristics conform to the SensorPath specification revision 0.98. Please refer to that speciation for further details.

| Symbol | Parameter | Conditions | Typical (Note 7) | Limits (Note 8) | Units (Limits) |
|---|---|---|---|---|---|
| **HARDWARE MONITOR CHARACTERISTICS** | | | | | |
| $t_{CONV}$ | Total Monitoring Cycle Time (Note 13) | All Voltage and Temperature readings (Default) | 182 | **163.8** | ms (min) |
| | | | | **200.2** | ms (max) |

## AC Electrical Characteristics (Continued)

The following specification apply for V+ = +3.0 $V_{DC}$ to +3.6 $V_{DC}$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$=0˚C to $T_{MAX}$=85˚C**; all other limits $T_A = T_J$ = 25˚C. The SensorPath Characteristics conform to the SensorPath specification revision 0.98. Please refer to that speciation for further details.

| Symbol | Parameter | Conditions | Typical (Note 7) | Limits (Note 8) | Units (Limits) |
|---|---|---|---|---|---|
| **SensorPath Bus CHARACTERISTICS** | | | | | |
| $t_f$ | SWD fall time (Note 16) | $R_{pull-up}$=1.25 kΩ ±30%, $C_L$=400 pF | | **300** | ns (max) |
| $t_r$ | SWD rise time (Note 16) | $R_{pull-up}$=1.25 kΩ ±30%, $C_L$=400 pF | | **1000** | ns (max) |
| $t_{INACT}$ | Minimum inactive time (bus at high level) guaranteed by the slave before an attention request | | | **11** | µs (min) |
| $t_{Mtr0}$ | Master drive for Data Bit 0 write and for Data Bit 0-1read | | | **11.8** | µs (min) |
| | | | | **17.0** | µs (max) |
| $t_{Mtr1}$ | Master drive for Data Bit 1 write | | | **35.4** | µs (min) |
| | | | | **48.9** | µs (max) |
| $t_{SFEdet}$ | Time allowed for LM41 activity detection | | | **9.6** | µs (max) |
| $t_{SLout1}$ | LM41 drive for Data Bit 1 read by master | | | **28.3** | µs (min) |
| | | | | **38.3** | µs (max) |
| $t_{MtrS}$ | Master drive for Start Bit | | | **80** | µs (min) |
| | | | | **109** | µs (max) |
| $t_{SLoutA}$ | LM41 drive for Attention Request | | | **165** | µs (min) |
| | | | | **228** | µs (max) |
| $t_{RST}$ | Master or LM41 drive for Reset | | | **354** | µs (min) |
| $t_{RST\_MAX}$ | Maximum drive of SWD by an LM41, after the power supply is raised above 3V | | | **500** | ms (max) |

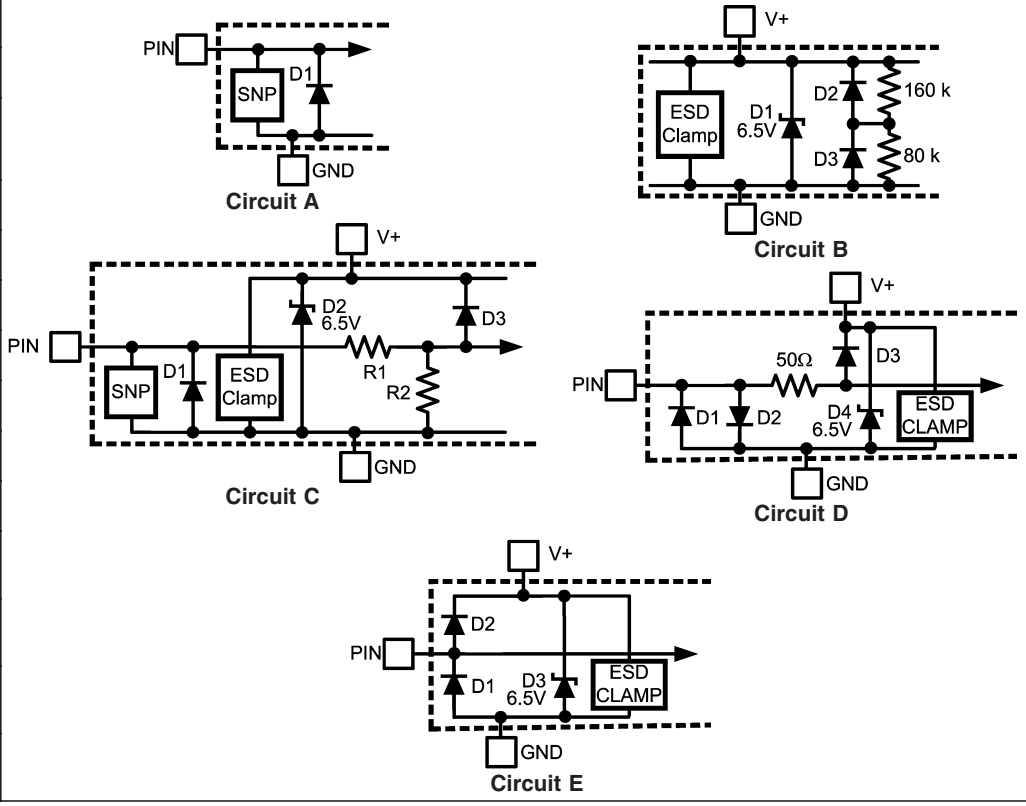
**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** All voltages are measured with respect to GND, unless otherwise noted.

**Note 3:** When the input voltage ($V_{IN}$) at any pin exceeds the power supplies ($V_{IN}$ < GND or $V_{IN}$ > V+), the current at that pin should be limited to 5 mA. Parasitic components and/or ESD protection circuitry are shown below for the LM41's pins. The nominal breakdown voltage of the zener is 6.5 V. SNP stands for snap-back device.

| PIN # | Pin Name | Pin Circuit |
|---|---|---|
| 1 | NC | A |
| 2 | GND | B |
| 3 | V+/ 3.3V SB | B |
| 4 | SWD | A |
| 5 | ADD | A |
| 6 | +1.2V | C |
| 7 | +2.5V | C |
| 8 | D- | D |
| 9 | D+ | E |
| 10 | NC | E |
| 11 | +5V | C |
| 12 | +12V | C |
| 13 | NC | none |
| 14 | NC | A |

**All Input Structure Circuits**




**Note 4:** Thermal resistance junction-to-ambient in still air when attached to a printed circuit board with 1 oz. foil is 148 ˚C/W.

**Note 5:** Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.

**Note 6:** Reflow temperature profiles are different for lead-free and non lead-free packages.

**Note 7:** "Typicals" are at $T_A$ = 25˚C and represent most likely parametric norm. They are to be used as general reference values not for critical design calculations.

**Note 8:** Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 9:** The supply current will not increase substantially with a SensorPath transaction.

**Note 10:** Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM41 and the thermal resistance. See (Note 4) for the thermal resistance to be used in the self-heating calculation.

**Note 11:** TUE , total unadjusted error, includes ADC gain, offset, linearity and reference errors. TUE is defined as the "actual Vin" to achieve a given code transition minus the "theoretical Vin" for the same code. Therefore, a positive error indicates that the input voltage is greater than the theoretical input voltage for a given code. If the theoretical input voltage was applied to an LM41 that has positive error, the LM41's reading would be less than the theoretical.

**Note 12:** The accuracy of the LM41CIMT is guaranteed when using the thermal diode of an Intel 90 nm Pentium 4 processor or any thermal diode with a non-ideality factor of 1.011 and series resistance of 3.33Ω. When using a MMBT3904 type transistor as a thermal diode the error band will be typically shifted by -4.5 ˚C.

**Note 13:** This specification is provided only to indicate how often temperature and voltage data are updated.

**Note 14:** The output fall time is measured from ($V_{IH\ min}$) to ($V_{IL\ max}$).

**Note 15:** The output rise time is measured from ($V_{IL\ max}$) to ($V_{IH\ min}$).

**Note 16:** The rise and fall times are not tested but guaranteed by design.

## Timing Diagrams

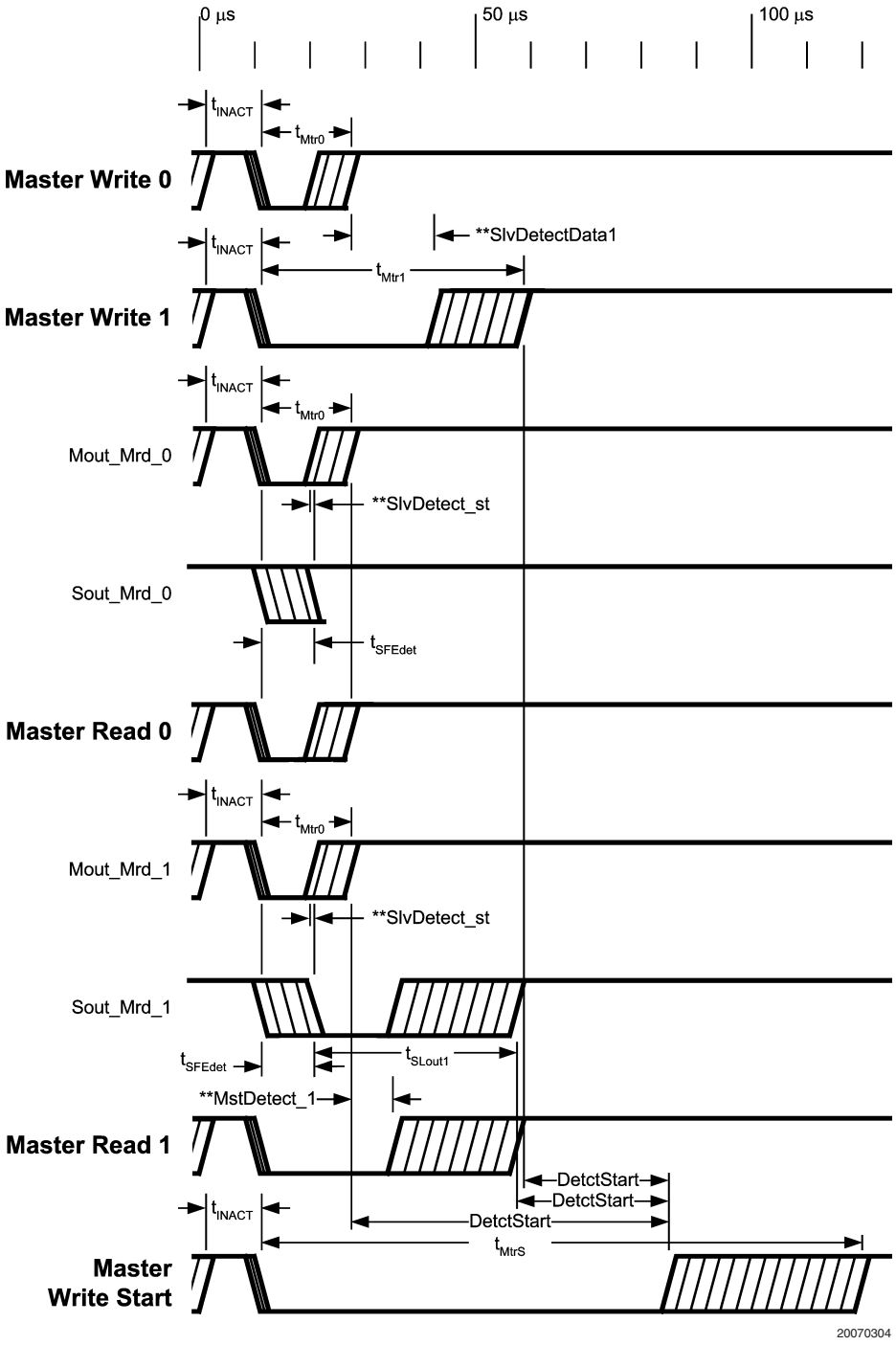



**FIGURE 1. Timing for Data Bits 0, 1 and Start Bit. See *Section 1.2* "SensorPath BIT SIGNALING" for further details.**

## Timing Diagrams (Continued)

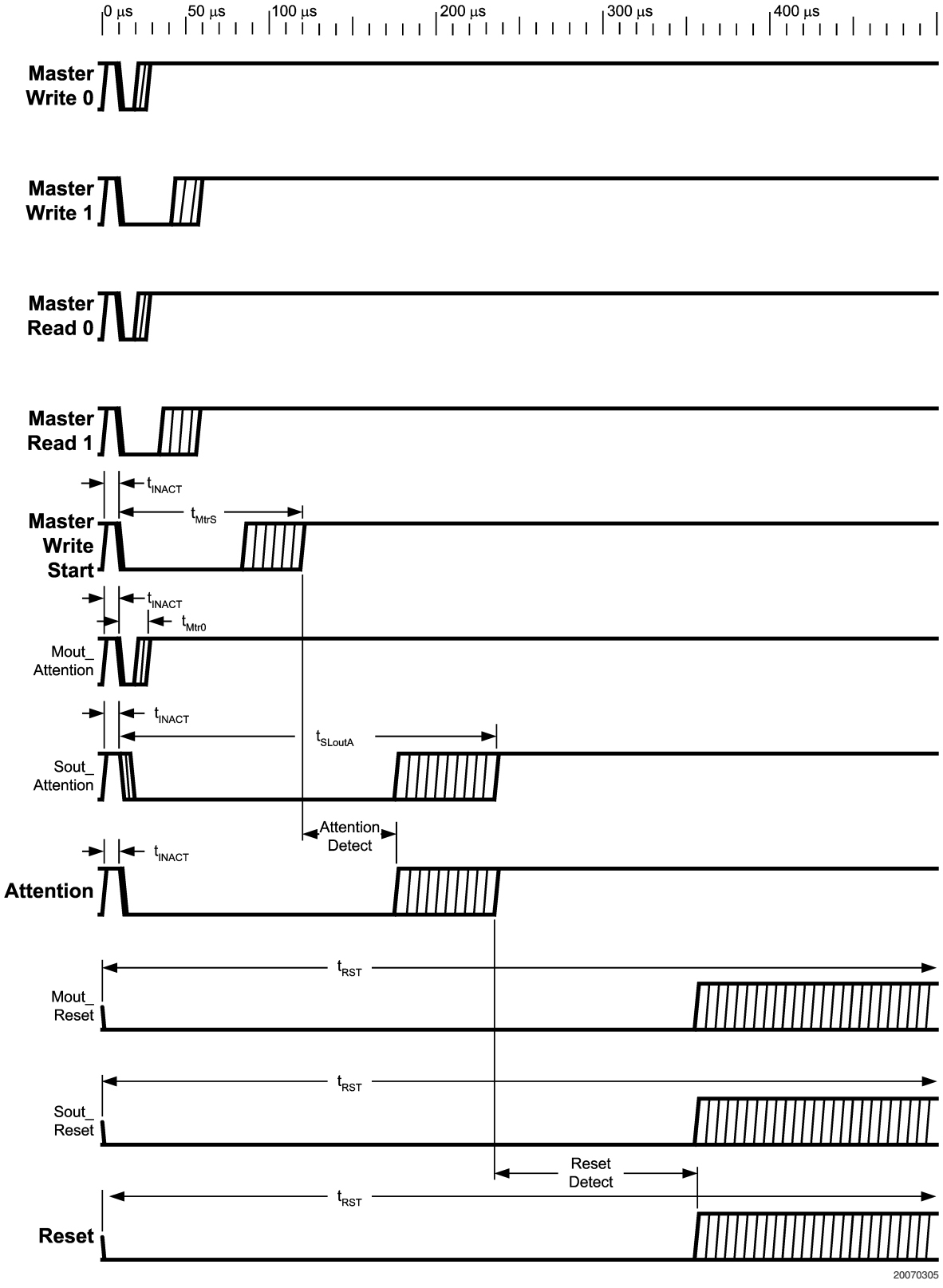
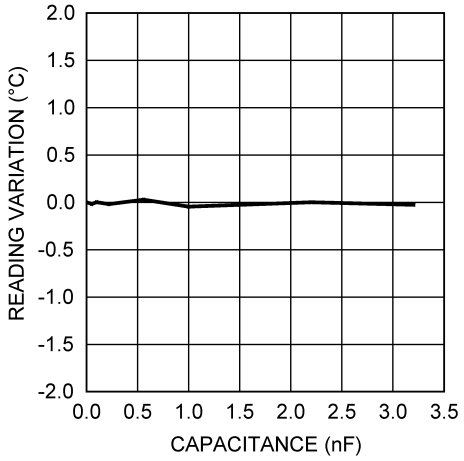



**FIGURE 2. Timing for Attention Request and Reset. See *Section 1.2* "SensorPath BIT SIGNALING" for further details.**

# Typical Performance Characteristics

**Remote Diode Temperature Reading Sensitivity to Diode Filter Capacitance**

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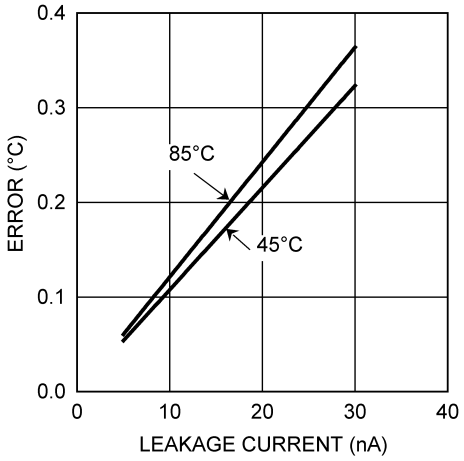
**Thermal Diode Capacitor or PCB Leakage Current Effect on Remote Diode Temperature Reading**

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# 1.0 Functional Description

The LM41 hardware monitor measures up to 2 temperature zones and 5 power supply voltages. The LM41 uses a $\Delta V_{be}$ temperature sensing method. A differential voltage, representing temperature, is digitized using a Sigma-Delta analog to digital converter. Internal scaling resistors allow direct measurement of the +1.6V, +2.5V, +5V, +3.3V and +12V power supply inputs. The digitized data can be retrieved over a simple single-wire interface called SensorPath. SensorPath has been defined by National Semiconductor and is optimized for hardware monitoring. National offers a royalty-free license in connection with its intellectual property rights in the SensorPath bus.

The LM41 has one address pin to allow up to two LM41s to be connected to one SensorPath bus. The physical interface of SensorPath's SWD signal is identical to the familiar industry standard SMBus SMBDAT signal. The digital information is encoded in the pulse width of the signal being transmitted. Every bit can be synchronized by the master simplifying the implementation of the master when using a micro-controller. For micro-controller's with greater functionality an asynchronous attention signal can be transmitted by the LM41 to interrupt the micro-controller and notify it that temperature/voltage data has been updated in the readout registers.

To optimize the LM41's power consumption to the system requirements, the LM41 has a shutdown mode and supports multiple conversion rates.

### 1.1 SensorPath BUS SWD

SWD is the Single Wire Data line used for communication. SensorPath uses 3.3V single-ended signaling, with a pull-up resistor and open-drain low-side drive (see *Figure 3*). For timing purposes SensorPath is designed for capacitive loads ($C_L$) of up to 400pF. Note that in many cases a 3.3V standby rail of the PC will be used as a power supply for both the sensor and the master. Logic high and low voltage levels for SWD are TTL compatible. The master may provide an internal pull-up resistor. In this case the external resistor is not needed. The minimum value of the pull-up resistor must take into account the maximum allowable output load current of 4mA.

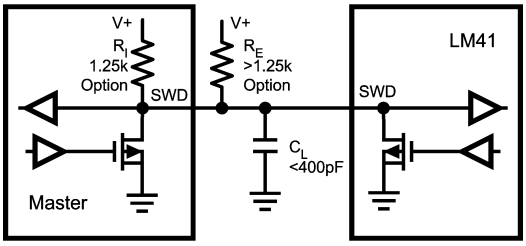


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**FIGURE 3. SensorPath SWD simplified schematic**

### 1.2 SensorPath BIT SIGNALING

Signals are transmitted over SensorPath using pulse-width encoding. There are five types of "bit signals":

- Data Bit 0
- Data Bit 1
- Start Bit
- Attention Request
- Reset

All the "bit signals" involve driving the bus to a low level. The duration of the low level differentiates between the different "bit-signals". Each "bit signal" has a fixed pulse width. SensorPath supports a Bus Reset Operation and Clock Training sequence that allows the slave device to synchronize its internal clock rate to the master. Since the LM41 meets the ±15% timing requirements of SensorPath, the LM41 does not require the Clock Training sequence and does not support this feature. This section defines the "bit signal" behavior in all the modes. Please refer to the timing diagrams in the Electrical Characteristics section (*Figure 1* and *Figure 2*) while going through this section. Note that the timing diagrams for the different types of "bit signals" are shown together to better highlight the timing relationships between them. However, the different types of "bit signals" appear on SWD at different points in time. These timing diagrams show the signals as driven by the master and the LM41 slave as well as the signal as seen when probing SWD. Signal labels that begin with the label Mout_ depict a drive by the master.

# 1.0 Functional Description (Continued)

Signal labels that begin with the label Slv_ depict the drive by the LM41. All other signals show what would be seen when probing SWD for a particular function (e.g. "Master Wr 0" is the Master transmitting a Data Bit with the value of 0).

### 1.2.1 Bus Inactive

The bus is inactive when the SWD signal is high for a period of at least $t_{INACT}$. The bus is inactive between each "bit signal".

### 1.2.2 Data Bit 0 and 1

All Data Bit signal transfers are started by the master. A Data Bit 0 is indicated by a "short" pulse; a Data Bit 1 is indicated by a longer pulse. The direction of the bit is relative to the master, as follows:

- Data Write - a Data Bit transferred from the master to the LM41.
- Data Read - a Data Bit transferred from the LM41 to the master.

A master must monitor the bus as inactive before starting a Data Bit (Read or Write).

A master initiates a data write by driving the bus active (low level) for the period that matches the data value ($t_{Mtr0}$ or $t_{Mtr1}$ for a write of "0" or "1", respectively). The LM41 will detect that the SWD becomes active within a period of $t_{SFEdet}$, and will start measuring the duration that the SWD is active in order to detect the data value.

A master initiates a data read by driving the bus for a period of $t_{Mtr0}$. The LM41 will detect that the SWD becomes active within a period of $t_{SFEdet}$. For a data read of "0", the LM41 will not drive the SWD. For a data read of "1" the LM41 will start within $t_{SFEdet}$ to drive the SWD low for a period of $t_{SLout1}$. Both master and LM41 must monitor the time at which the bus becomes inactive to identify a data read of "0" or "1".

During each Data Bit, both the master and all the LM41s must monitor the bus (the master for Attention Request and Reset; the LM41s for Start Bit, Attention Request and Reset) by measuring the time SWD is active (low). If a Start Bit, Attention Requests or Reset "bit signal" is detected, the current "bit signal" is not treated as a Data Bit.

Note that the bit rate of the protocol varies depending on the data transferred. Thus, the LM41 has a value of "0" in reserved or unused register bits for bus bandwidth efficiency.

### 1.2.3 Start Bit

A master must monitor the bus as inactive before beginning a Start Bit.

The master uses a Start Bit to indicate the beginning of a transfer. LM41s will monitor for Start Bits all the time, to allow synchronization of transactions with the master. If a Start Bit occurs in the middle of a transaction, the LM41 being addressed will abort the current transaction. In this case the transaction is not "completed" by the LM41 (see *Section 1.3* "SensorPath Bus Transactions").

During each Start Bit, both the master and all the LM41s must monitor the bus for Attention Request and Reset, by measuring the time SWD is active (low). If an Attention Request or Reset condition is detected, the current "bit signal" is not treated as a Start Bit. The master may attempt to send the Start Bit at a later time.

### 1.2.4 Attention Request

The LM41 may initiate an Attention Request when the SensorPath bus is inactive.

Note that a Data Bit, or Start Bit, from the master may start simultaneously with an Attention Request from the LM41. In addition, two LM41s may start an Attention Request simultaneously. Due to its length, the Attention Request has priority over any other "bit signal", except Reset. Conflict with Data Bits and Start Bits are detected by all the devices, to allow the bits to be ignored and re-issued by their originator.

The LM41 will either check to see that the bus is inactive before starting an Attention Request, or start the Attention Request within the $t_{SFEdet}$ time interval after SWD becomes active. The LM41 will drive the signal low for $t_{SLoutA}$ time. After this, both the master and the LM41 must monitor the bus for a Reset Condition. If a Reset condition is detected, the current "bit signal" is not treated as an Attention Request.

After Reset, an Attention Request can not be sent before the master has sent 14 Data Bits on the bus. See *Section 1.3.5* for further details on Attention Request generation.

### 1.2.5 Bus Reset

The LM41 issues a Reset at power up. The master must also generate a Bus Reset at power-up for at least the minimum reset time, it must not rely on the LM41. SensorPath puts no limitation on the maximum reset time of the master. Following a Bus Reset, the LM41 may generate an Attention Request only after the master has sent 14 Data Bits on the bus. See *Section 1.3.5* for further details on Attention Request generation.

### 1.3 SensorPath BUS TRANSACTIONS

SensorPath is designed to work with a single master and up to seven slave devices. Each slave has a unique address. The LM41 supports up to 2 device addresses that are selected by the state of the address pin ADD. The Register Set of the LM41 is defined in *Section 2.0*.

### 1.3.1 Bus Reset Operation

A Bus Reset Operation is global on the bus and affects only the communication interface of all the devices connected to it. The Bus Reset operation does not affect either the contents of the device registers, or device operation, to the extent defined in LM41 Register Set, see *Section 2.0*.

The Bus Reset operation is performed by generating a Reset signal on the bus. The master must apply Reset after power-up, and before it starts operation. The Reset signal end will be monitored by all the LM41s on the bus.

After the Reset Signal the SensorPath specification requires that the master send a sequence of 8 Data Bits with a value of "0", without a preceding Start Bit. This is required to enable slaves that "train" their clocks to the bit timing. The LM41 does not require nor does it support clock training.

# 1.0 Functional Description (Continued)

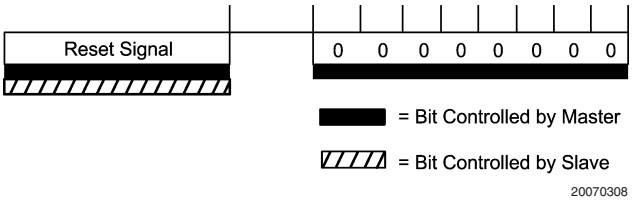



**FIGURE 4. Bus Reset Transaction**

### 1.3.2 Read Transaction

During a read transaction, the master reads data from a register at a specified address within a slave. A read transaction begins with a Start Bit and ends with an ACK bit, as shown in *Figure 5*.

- **Device Number** This is the address of the LM41 device accessed. Address "000" is a broadcast address and can be responded to by all the slave devices. The LM41 ignores the broadcast address during a read transaction.
- **Internal Address** The address of a register within the LM41 that is read.
- **Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$)** A "1" indicates a read transaction.
- **Data Bits** During a read transaction the data bits are driven by the LM41. Data is transferred serially with the most significant bit first. This allows throughput optimization based on the information that needs to be read.

  The LM41 supports 8-bit or 16-bit data fields, as described in *Section 2.0* "Register Set".
- **Even Parity (EP)** This bit is based on all preceding bits (device number, internal address, Read/$\overline{\text{Write}}$ and data bits) and the parity bit itself. The parity -number of 1's - of all the preceding bits and the parity bit must be even - i.e., the result must be 0. During a read transaction, the EP bit is sent by the LM41 to the master to allow the master to check the received data before using it.
- **Acknowledge (ACK)** During a read transaction the ACK bit is sent by the master indicating that the EP bit was received and was found to be correct, when compared to the data preceding it, and that no conflict was detected on the bus (excluding Attention Request - see *Section 1.3.5* "Attention Request Transaction"). A read transfer is considered "complete" only when the ACK bit is received. A transaction that was not positively acknowledged is not considered "complete" by the LM41 and following are performed:

  — The BER bit in the LM41 Device Status register is set

  — The LM41 generates an Attention Request before, or together with the Start Bit of the next transaction

  A transaction that was not positively acknowledged is also not considered "complete" by the master (i.e. internal operations related to the transaction are not performed). The transaction may be repeated by the master, after detecting the source of the Attention Request (the LM41 that has a set BER bit in the Device Status register). Note that the SensorPath protocol neither forces, nor automates re-execution of the transaction by the master.

  The values of the ACK bit are:

  — 1: Data was received correctly

  — 0: An error was detected (no-acknowledge).

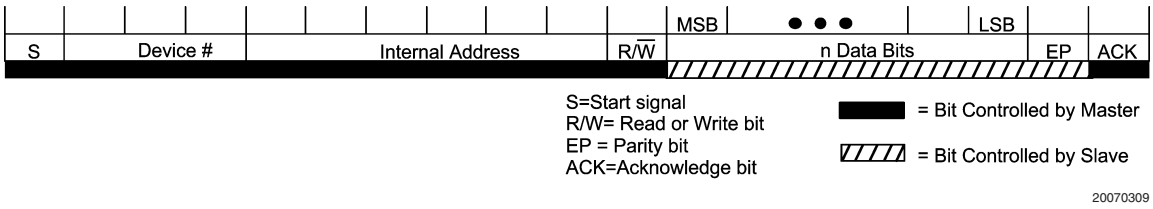



**FIGURE 5. Read Transaction, master reads data from LM41**

### 1.3.3 Write Transaction

In a write transaction, the master writes data to a register at a specified address in the LM41. A write transaction begins with a Start Bit and ends with an ACK Data Bit, as show in *Figure 6*.

- **Device Number** This is the address of the slave device accessed. Address "000" is a broadcast address and is responded to by all the slave devices. The LM41 responds to broadcast messages to the Device Control Register.
- **Internal Address** This is the register address in the LM41 that will be written.
- **Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$)** A "0" data bit directs a write transaction.

# 1.0 Functional Description (Continued)

- **Data Bits** This is the data written to the LM41 register, are driven by the master. Data is transferred serially with the most significant bit first. The number of data bits may vary from one address to another, based on the size of the register in the LM41. This allows throughput optimization based on the information that needs to be written.

  The LM41 supports 8-bit or 16-bit data fields, as described in *Section 2.0* "Register Set".
- **Even Parity (EP)** This data bit is based on all preceding bits (Device Number, Internal Address, Read/Write and Data bits) and the Even Parity bit itself. The parity (number of 1's) of all the preceding bits and the parity bit must be even - i.e. the result must be 0. During a write transaction, the EP bit is sent by the master to the LM41 to allow the LM41 to check the received data before using it.
- **Acknowledge (ACK)** During the write transaction the ACK bit is sent by the LM41 indicating to the master that the EP was received and was found correct, and that no conflict was detected on the bus (excluding Attention Request - see *Section 1.3.5* "Attention Request Transaction"). A write transfer is considered "completed" only when the ACK bit is generated. A transaction that was not positively acknowledged is not considered complete by the LM41 (i.e. internal operation related to the transaction are not performed) and the following are performed:

  — The BER bit in the LM41 Device Status register is set;

  — The LM41 generates an Attention Request before, or together with the Start Bit of the next transaction

  A transaction that was not positively acknowledged is also not considered "complete" by the master (i.e. internal operations related to the transaction are not performed). The transaction may be repeated by the master, after detecting the source of the Attention Request (the LM41 that has a set BER bit in the Device Status register). Note that the SensorPath protocol neither forces, nor automates re-execution of the transaction by the master.

  The values of the ACK bit are:

  — 1: Data was received correctly;

  — 0: An error was detected (no-acknowledge).

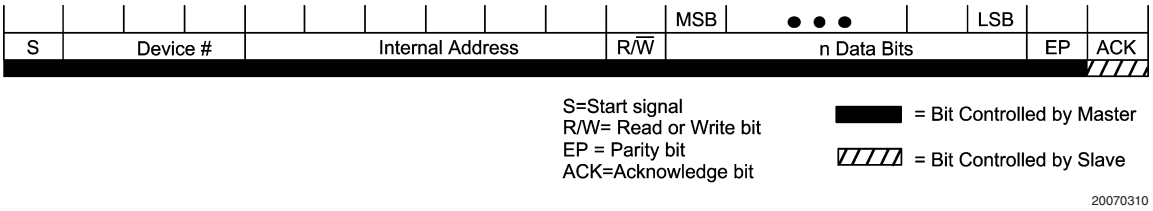



**FIGURE 6. Write Transaction, master write data to LM41**

### 1.3.4 Read and Write Transaction Exceptions

This section describes master and LM41 handling of special bus conditions, encountered during either Read or Write transactions.

If an LM41 receives a Start Bit in the middle of a transaction, it aborts the current transaction (the LM41 does not "complete" the current transaction) and begins a new transaction. Although not recommend for SensorPath normal operation, this situation is legitimate, therefore it is not flagged as an error by the LM41 and Attention Request is not generated in response to it. The master generating the Start Bit, is responsible for handling the not "complete" transaction at a "higher level".

If LM41 receives more than the expected number of data bits (defined by the size of the accessed register), it ignores the unnecessary bits. In this case, if both master and LM41 identify correct EP and ACK bits they "complete" the transaction. However, in most cases, the additional data bits differ from the correct EP and ACK bits. In this case, both the master and the LM41 do not "complete" the transaction. In addition, the LM41 performs the following:

- the BER bit in the LM41 Device Status register is set
- the LM41 generates an Attention Request

If the LM41 receives less than the expected number of data bits (defined by the size of the accessed register), it waits indefinitely for the missing bits to be sent by the master. If then the master sends the missing bits, together with the correct EP/ACK bits, both master and LM41 "complete" the transaction. However, if the master starts a new transaction generating a Start Bit, the LM41 aborts the current transaction (the LM41 does not "complete" the current transaction) and begins the new transaction. The master is not notified by the LM41 of the incomplete transaction.

### 1.3.5 Attention Request Transaction

Attention Request is generated by the LM41 when it needs the attention of the master. The master and all LM41s must monitor the Attention Request to allow bit re-sending in case of simultaneous start with a Data Bit or Start Bit transfer. Refer to the "Attention Request" section, *Section 1.2.4* in the "Bit Signaling" portion of the data sheet.

The LM41 will generate an Attention Request using the following rules:

1. A Function event that sets the Status Flag has occurred and Attention Request is enabled **and**
2. The "physical" condition for an Attention Request is met (i.e., the bus is inactive), **and**
3. At the first time 2 is met after 1 occurred, there has not been an Attention request on the bus since a read of the Device Status register, **or** since a Bus Reset.

**OR**

1. A bus error event occurred, **and**
2. the "physical" condition for an Attention Request is met (i.e., the bus is inactive), **and**
3. At the first time 2. is met after 1 occurred, there has not been a Bus Reset.

## 1.0 Functional Description (Continued)

All devices (master or slave) must monitor the bus for an Attention Request signal. The following notes clarify the intended system operation that uses the Attention Request Indication.

- Masters are expected to use the attention request as a trigger to read results from the LM41. This is done in a sequence that covers all LM41s. This sequence is referred to as "master sensor read sequence".
- After an Attention Request is sent by an LM41 until after the next read from the Device Status register the LM41 does not send Attention Requests for a function event since it is guaranteed that the master will read the Status register as part of the master sensor read sequence. Note that the LM41 will send an attention for BER, regardless of the Status register read, to help the master with any error recovery operations and prevent deadlocks.
- A master must record the Attention Request event. It must then scan all slave devices in the system by reading their Device Status register and must handle any pending event in them before it may assume that there are no more events to handle.

Note: there is no indication of which slave has sent the request. The requirement that multiple requests are not sent allows the master to know within one scan of register reads that there are no more pending events.

#### 1.3.6 Fixed Device Number Setting

The LM41 device number is defined by strapping of the ADD pin. The LM41 will wake (after Device Reset) with the Device Number field of the Device Number register set to the address as designated in *Section 2.3* "Device Number". It is the responsibility of the system designer to avoid having two devices with the same Device Number on the bus.

Devices should be detected by the master by a read operation of the Device Number register. The read returns "000" if there is no device at that address on the bus (the EP bit must be ignored).

# 2.0 Register Set

## 2.1 REGISTER SET SUMMARY

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 000 00h | Device Number | R | * | Not Available | | | | | | | | Reserved | | | | | See *Section 2.3* | | |
| | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | | | |
| 000 001 01h | Manufacturer ID | R | 100Bh | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 000 010 02h | Device ID | R | 24h | RevID | | | | | Device ID | | | | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 000 011 03h | Capabilities Fixed | R | 21h | Reserved | | | | | | | | FuncDescriptor 2 (Voltage-Only) | | | | FuncDescriptor 1 (Temperature) | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 000 100 04h | Device Status | R | 0h | Not Available | | | | | | | | BER | Res 0 | ERF2 | ERF1 | Reserved 0 0 | | SF2 | SF1 |
| 000 101 05h | Device Control | R/W | 0h | Reserved | | | | | | | | | | EnF2 | EnF1 | Res | Low Pwr | Shut down | Reset |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | 0 | | | |
| 001 000 08h | Temperature Capabilities | R | 0349h | Reserved | | | | # of Remotes | | | Int Sens | Rout Size | Sign | 10-Bits | | | 0.5˚C Resolution | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 001 001 09h | Processor/ Remote Temperature Data Readout | R | | MSb Sign | 128 ˚C | 64˚C | 32˚C | 16˚C | 8˚C | 4˚C | 2˚C | 1 ˚C | LSb 0.5 ˚C | Res 0 0 0 | | | S NUM | EF | Res 0 |
| | Local Temperature Data Readout | | | | | | | | | | | | | Res 0 0 0 | | | | Res 0 | Res 0 |
| 001 010 0Ah | Temperature Control | R/W | 0h | Reserved | | | | | | | | | | | | | EN1 | EN0 | ATE |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 001 011 -001 111 0Bh-0Fh | Reserved | R | | Undefined | | | | | | | | | | | | | | | |
| 010 000 10h | Voltage Capabilities | R | 0051h | Reserved | | | | | | | # of Voltage Sensors | | | | | Rout Size | Resolution 9-Bits | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 010 001 11h | Voltage Readout | R | | Voltage Readout | | | | | | | | | Reserved | | SNUM | | Reserved | | |
| | | | | MSb | | | | | | | | LSb | 0 | 0 | | | | 0 | 0 |
| 010 010 12h | Voltage Control | R/W | 1Fh | Reserved | | | | | EN4 | EN3 | EN2 | EN1 | EN0 | ATE | Low Rate Function (Read Only) | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | | | | | | | 1 | 1 | 1 | 1 | 1 |
| 010 011 -011 111 13h-1Fh | Reserved | R | | Undefined | | | | | | | | | | | | | | | |
| 100 000 20h | Conversion Rate | R/W | 2h | Not Available | | | | | | | | Reserved | | | | | | CR1 | CR0 |
| | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 100 001 -111 111 21h-3Fh | Undefined Registers | R | | Undefined | | | | | | | | | | | | | | | |

## 2.0 Register Set (Continued)

* Depends on state of ADD pins see *Section 2.3* "Device Number".

### 2.2 DEVICE RESET OPERATION

A Device Reset operation is performed in the following conditions:

- At device power-up.
- When the Reset bit in the Device Control register is set to 1 (see *Section 2.8* "Device Control").

The Device Reset operation performs the following:

- Aborts any device operation in progress and restarts device operation.
- Sets all device registers to their "Reset" (default) value.

### 2.3 DEVICE NUMBER (Addr: 000 000; 00h)

This register is used to specify a unique address for each device on the bus.

| Reg Add | Register Name | R/W | POR Val | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 000 | Device Number | R | 7h or 1h | Reserved | | | | | AS2 | AS1 | AS0 |
| | | | | 0 | 0 | 0 | 0 | 0 | | | |

The value of [AS2:AS0] is determined by the setting of the ADD input pin:

**TABLE 1. Device Number Assignment**

| ADD | [AS2:AS0] |
|---|---|
| 0 | 001 |
| 1 | 111 |

The value of [AS2:AS0] will directly change and follow the value determined by ADD. Since this is a read only register the value of the address cannot be changed by software.

### 2.4 MANUFACTURER ID (Addr: 000 001; 01h)

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 001 | Manufacturer ID | R | 100Bh | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

The manufacturer ID matches that assigned to National Semiconductor by the PCI SIG. This register may be used to identify the manufacturer of the device in order to perform manufacturer specific operations.

## 2.0 Register Set (Continued)

### 2.5 DEVICE ID (Addr: 000 010; 02h)

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 010 | Device ID | R | 24h | RevID | | | | | DeviceID | | | | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |

The device ID is defined by the manufacturer of the device and is unique for each device produced by a manufacturer. Bits 15-11 identify the revision number of the die and will be incremented upon revision of the device.

| Bit | Type | Description |
|---|---|---|
| 10-0 | RO | **DeviceID (Device ID Value)** A fixed value that identifies the device. |
| 15-11 | RO | **RevID (Revision ID Value)** A fixed value that identifies the device revision. |

### 2.6 CAPABILITIES FIXED (Addr: 000 011; 03h)

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 011 | Capabilities Fixed | R | 21h | Reserved | | | | | | | | FuncDescriptor2 | | | | FuncDescriptor1 | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

The value of this register defines the capabilities of the LM41. The LM41 supports two functions, that of Temperature Measurement type (Function 1) and Voltage-Only Measurement type (Function 2). Please refer to the SensorPath specification for further details on other FuncDescriptor values.

### 2.7 DEVICE STATUS (Addr: 000 100; 04h)

This register is set to the reset value by a Device Reset.

| Reg Add | Register Name | R/W | POR Val | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 100 | Device Status | R | 0h | BER | Res | ERF2 | ERF1 | Res | | SF2 | SF1 |
| | | | | | 0 | | | 0 | 0 | | |

| Bit | Type | Description |
|---|---|---|
| 0 | RO | **SF1 (Status Function 1)** This bit is set by a Function Event within Function 1. Event details are function dependent and are described within the function. SF1 is cleared by Device Reset or by handling the event within the Temperature Measurement Function (see *Section 2.9* for further details).<br>0: Status flag for Function 1 is inactive (no event).<br>1: Status flag for Function 1 is active indicating that a Function Event has occurred. |
| 1 | RO | **SF2 (Status Function 2)** Same as SF1 for Function 2, Voltage-Only Measurement Function. (see *Section 2.10* for further details) |
| 3-2 | RO | **Reserved.** Will always read "0". |
| 4 | RO | **ERF1 (Error Function 1)** This bit is set in response to an error indication within Function 1. ERF1 is cleared by Device Reset or by handling the error condition within the Temperature Measurement Function (see *Section 2.9* for further details).<br>0: No error occurred in Function 1.<br>1: Error occurred in Function 1. |
| 5 | RO | **ERF2 (Error Function 2)** Same as ERF1 for Function 2, Voltage-Only Measurement Function. (see *Section 2.10* for further details) |
| 6 | RO | **Reserved.** Will always read "0". |

## 2.0 Register Set (Continued)

| Bit | Type | Description |
|---|---|---|
| 7 | RO | **BER (Bus Error)** This bit is set when the device either generates, or receives an error indication in the ACK bit of the transaction (i.e., no-acknowledge). BER is cleared by Device Reset or by reading the Device Status register.<br>0: No transaction error occurred.<br>1: An ACK bit error (no-acknowledge) occurred during the last transaction. |

### 2.8 DEVICE CONTROL (Addr: 000 101; 05h)

This register responds to a broadcast write command (Device Number 000). Write using broadcast address is ignored by bits 15-2. This register is set to the reset value by a Device Reset.

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 101 | Device Control | R/W | 0h | Reserved | | | | | | | | | | EnF2 | EnF1 | Res | Low Pwr | Shut down | Reset |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | |

| Bit | Type | Description |
|---|---|---|
| 0 | R/W | **Reset (Device Reset).** When set to "1" this bit initiates a Device Reset operation ( See *Section 2.2*). This bit self-clears after the Device Reset operation is completed.<br>0: Normal device operation. (default)<br>1: Device Reset<br>The LM41 does not require a Device Reset command after power. |
| 1 | R/W | **Shutdown (Shutdown Mode).** When set to "1" this bit stops the operation of all functions and places the device in the lowest power consumption mode.<br>0: Device in Active Mode. (default)<br>1: Device in Shutdown Mode. |
| 2 | R/W | **LowPwr (Low-Power Mode).** When set to "1" this bit slows the operation of all functions and places the device in a low power consumption mode. In Low-Power Mode, the conversion rate of the LM41 is effected see *Section 2.11* for further details.<br>0: Device in Active Mode. (default)<br>1: Device in Low-Power Mode. |
| 3 | RO | **Not supported.** Will always read "0". |
| 4 | R/W | **EnF1 (Enable Function 1).** When bit is set to "1" this bit Function 1 is enabled for operation. A function may require setup before this bit is set. The function registers can be accessed even when the function is disabled.<br>0: Function 1 is disabled. (default)<br>1: Function is enabled. |
| 5 | R/W | **EnF2 (Enable Function 2).** Same as EnF1 for Function 2. |
| 15-6 | RO | **Not supported.** Will always read "0". |

### 2.9 TEMPERATURE MEASUREMENT FUNCTION (TYPE - 0001)

This section defines the register structure and operation of a Temperature Measurement function as it applies to the LM41. The FuncDescriptor value of this function is '0001'.

#### 2.9.1 Operation

The Temperature Measurement function as implemented in the LM41 supports 2 temperature zones, the LM41's internal temperature (LM41's junction temperature) and the remote temperature of a thermal diode (stand alone transistors or integrated in chips). The function measures multiple temperature points and reports the readout to the master. The measurement of all the enabled temperature sensors is cyclic and continuous.

**Sensor Scan** The Control register of the function defines which temperature sensors are included in the scan. A sensor is scanned only if it is enabled by the Sensor Enable bits (EN0 and EN1). The sensors are scanned in an ascending, round-robin order, based on the sensor number. Disabled sensors are skipped and the next enabled sensor in ascending order is scanned.

## 2.0 Register Set (Continued)

The minimum scan rate is recommended to be 4Hz (i.e. the measurement data is updated at least once in 250 ms), see *Section 2.11* for further details. In Low-Power Mode, the scan rate is four times lower than the scan rate in Active Mode. The scan rate effects the bus bandwidth required to read the results. The sampling rate of the temperature measurements can also be controlled via the Conversion Rate register, see *Section 2.11* for further details.

**Data Readout** When a new result is stored in the Readout register a Function Event is generated. Reading the Readout register clears the Status Function 1 flag (SF1). The result is available in the Readout register waiting for the master to read it during the master sensor read sequence. If a new result is ready before the previous result has been read, the new result overwrites the previous result and the Error Function 1 flag (ERF1) is set (indicating an overrun event). Reading the Readout register clears also the Error Function 1 flag (ERF1). The Readout register contains the temperature data, and the sensor number. Since the LM41 only supports three temperature zones the sensor number field will be zero to two. Other fields in the Readout register as defined by the SensorPath specification are not supported.

**Readout Resolution** The resolution of the readout is defined in the Temperature Capabilities register. The resolution of the LM41 is fixed and cannot be modified by software. The temperature readout type is common to all the sensors and is signed two's complement fixed point value. The readout type is specified in the Capabilities register of the function.

Sensor 0 in the Temperature Measurement function is reserved for local temperature measurement (i.e., the junction temperature of the LM41).

**Function Event** The Temperature Measurement function generates a Function Event whenever a conversion cycle is completed and new data is stored in the Readout Register. When the new data is stored into the Readout register the SF1 bit in the device Status register is set to "1" and remains set, until it is cleared by reading the Readout register. An Attention Request is generated on the bus, only if it is enabled by the Attention Enable bit (ATE) in the Temperature Control register.

**Setup Before Enabling** No setup is required for the Temperature Measurement function before the function is enabled.

#### 2.9.2 Temperature Capabilities (Addr: 001 000; 08h)

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 001 000 | Temperature Capabilities | R | 0349h | Reserved | | | | # of Remotes | | | Int Sens | Rout Size | Sign | 10-Bits | | | 0.5˚C Resolution | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

This register defines the format of the temperature data in the readout register. The LM41 only supports one format for all temperatures as defined by the values of this register.

| Bit | Type | Description |
|---|---|---|
| 2-0 | RO | **Resolution.** This field defines the value of 1 LSb of the Temperature Readout field in the Readout Register. The SensorPath specification defines many different weights for the temperature LSb. The LM41 supports a resolution of 0.5 ˚C and thus a value of 001 for this field. For a full definition of this field, please refer to the SensorPath specification. |
| 5-3 | RO | **Number of Bits.** This field defines the total number of significant bits of the Temperature Readout field in the Readout register. The total number of significant bits includes the number of bits representing the integer part of the temperature data and the fractional part of it, as defined by the Resolution field. The LM41 supports 10-bits and thus a value of 001 for this field. For a full definition of this field please refer to the SensorPath specification. |
| 6 | RO | **Sign (Signed Data).** Defines the type of data in the Temperature Readout field of the Readout register.<br>0: Unsigned, positive fixed point value.<br>1: Signed, 2's complement fixed point value. (value for the LM41) |
| 7 | RO | **RoutSize (Readout Register size).** Defines the total size of the Readout register.<br>0: 16 bits. (value for the LM41) |
| 8 | RO | **IntSens (Internal Sensor Support).** Indicates if the device supports internal temperature measurements, as the LM41 does.<br>0: No internal temperature measurement<br>1: Internal temperature sensor implemented. (value for the LM41) |
| 11-9 | RO | **# of Remotes (Number of Remote Sensors).** Specifies the number of remote Temperature Sensors supported by the function.<br>1: The number of Remote Temperature Sensors. (value for the LM41) |
| 15-12 | RO | **Reserved.** Will always read "0". |

## 2.0 Register Set (Continued)

**2.9.3 Temperature Data Readout (Addr: 001 001; 09h)**

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 001 001 | Local Temperature Data Readout | R | | MSb Sign | 128 ˚C | 64˚C | 32˚C | 16˚C | 8˚C | 4˚C | 2˚C | 1˚C | 0.5 ˚C | Reserved | | | S NUM | Reserved | |
| | | | | | | | | | | | | | | 0 | 0 | 0 | | 0 | 0 |
| | Processor/ Remote Temperature Data Readout | | | | | | | | | | | | | Reserved | | | | EF | Res |
| | | | | | | | | | | | | | | 0 | 0 | 0 | | | 0 |

| Bit | Type | Description |
|---|---|---|
| 0 | RO | **Reserved.** Will always read "0". |
| 1 | RO | **Reserved for Local Temperature Data Readout.** Will always read "0".<br>**EF (Error Flag) for Remote Temperature Data Readout.** This bit indicates that an error was detected during the measurement of the current remote Temperature sensor such as a diode fault condition. When a diode fault occurs the value of the temperature reading will be 200h or -256˚C.<br>0: No error detected.<br>1: Error detected. |
| 2 | RO | **SNUM (Sensor Number).** This field indicates the number of the current Temperature Sensor, to which the data in the Temperature Readout field belongs. Temperature Sensor 0 is always assigned to the local sensor of the LM41.<br>0: Local temperature sensor (see *Table Thermal Diode Input Mapping*)<br>1: Remote sensor (see *Table Thermal Diode Input Mapping*) |
| 5-3 | RO | **Reserved.** Will always read "0". |
| 15-6 | RO | **Temperature Readout.** This field holds the result of the temperature measurement. The active size of this field for the LM41 is 10-bits, left justified. See *Table Temperature Data Format* for examples. |

**Thermal Diode Input Mapping**

| Sensor Number (SNUM) | Sensor Input | Board Connection |
|---|---|---|
| 0 | Local | none |
| 1 | Processor, D+/D- | CPU Thermal Diode, MMBT3904 Thermal Diode or GPU Thermal Diode |

All LM41 temperature data has a common format. The LM41's temperature data format is two's complement and has 10-bits of resolution with the LSb having a weight of 0.5 ˚C. The LM41 can resolve temperature between +255.5 ˚C and -256 ˚C, inclusive. It can measure local temperatures between +85 ˚C and 0 ˚C and remote temperatures between +125 ˚C and 0 ˚C with an accuracy of ±3.0 ˚C.

**Temperature Data Format**

| Temperature | Binary | Hex |
|---|---|---|
| +140 ˚C | 01 0001 1000 | 118h |
| +100 ˚C | 00 1100 1000 | 0C8h |
| +1 ˚C | 00 0000 0010 | 002h |
| 0 ˚C | 00 0000 0000 | 000h |
| - 0.5 ˚C | 11 1111 1111 | 3FFh |
| -1 ˚C | 11 1111 1110 | 3FEh |
| - 40 ˚C | 11 1011 0000 | 3B0h |

## 2.0 Register Set (Continued)

**Temperature Data Format** (Continued)

| Temperature | Binary | Hex |
|---|---|---|
| -255.5 ˚C | 10 0000 0001 | 201h |
| -256 ˚C | 10 0000 0000 | 200h |

### 2.9.4 Temperature Control (Addr: 001 010; 0Ah)

This register is set to the reset value by a Device Reset.

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 001 010 | Temperature Control | R/W | 0h | Reserved | | | | | | | | | | | | | EN1 | EN0 | ATE |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

| Bit | Type | Description |
|---|---|---|
| 0 | R/W | **ATE (Attention Enable).** When set, this bit enables an Attention Request signal to be generated by the LM41, if the EN0, EN1 or EN2 bits of this register are set.<br>0: Attention Request disabled (from enabled Temperature Sensor- default)<br>1: Attention Request enabled (from enabled Temperature Sensor) |
| 1 | R/W | **EN0 (Enable Sensor 0).** When this bit is set, the Local Temperature Sensor is enabled for temperature measurements.<br>0: Temperature Sensor disabled (default)<br>1: Temperature Sensor enabled |
| 2 | R/W | **EN1 (Enable Sensor).** When this bit is set, the Remote Thermal Diode Temperature Sensor is enabled for temperature measurements.<br>0: Temperature Sensor disabled (default)<br>1: Temperature Sensor enabled |
| 15-3 | RO | **Reserved.** Will always read "0". |

### 2.10 VOLTAGE-ONLY MEASUREMENT FUNCTION (TYPE 0010)

This section defines the register structure and operation of the Voltage-Only Measurement Function. The FuncDescriptor value of this function is ‘0010’.

### 2.10.1 Operation

The Voltage-Only measurement function is capable of measuring the voltage of voltage measurement points ("sensors"). These may be general or dedicated inputs (e.g., for backup battery measurement or the supply voltage to the device). The measurement of all the enabled voltage sensors is cyclic and continuous.

**Sensor Scan** The control register of the function defines which voltage sensors (inputs) are included in the scan. A sensor is scanned only if it is enable by the Sensor Enable bit (EN0, EN1, EN2, EN3 and EN4). The sensors are scanned in an ascending, round-robin order, based on the sensor number. Disable sensors are skipped and the next enabled sensor in ascending order is scanned.

The minimum scan rate is recommended to be 4Hz (i.e., the measurement data is updated at least once in 250 ms), see *Section 2.11* for further details. In Low-Power Mode, the scan rate is four times lower than the scan rate in Active Mode. The scan rate effects the bus bandwidth required to read the results. The sampling rate of the voltage measurements can also be controlled via the Conversion Rate register, see *Section 2.11* for further details.

**Data Readout** When a new result is stored in the Readout register a Function Event is generated. Reading the Readout register clears the Status Function 2 flag (SF2) for the Voltage-Only Measurement Function in the Device Status register. The result is available in the Readout register waiting for the master to read it during the master sensor read sequence. The device should delay or buffer additional conversions to allow the master time to read the result (see Sensor Scan Rate *Section 2.11*). If a new result is ready before the previous result has been read, the new results overwrites the previous result and the Error Function 2 flag (ERF2) for the Voltage-Only function in the Device Status register is set (indicating an overrun event). Reading the Voltage-Only Measurement Readout register clears also the ERF2 flag.

**Readout Resolution** The resolution of the readout register is defined in the Voltage Capabilities register. The resolution of the LM41 is fixed and cannot be modified by software. The voltage readout format is common to all voltage sensors and is 9-bits unsigned. For over or under input voltage conditions the data is guaranteed to saturate at all "1"s or "0"s so long as Operating Ratings of the LM41 are adhered to.

## 2.0 Register Set (Continued)

**Function Event** The Voltage-Only Measurement function generates a Function Event to the master whenever a conversion cycle is completed and new data is stored in the Readout register. When the new data is stored into the Readout register the SF2 bit in the Device Status register is set to 1 and remains set, until it is cleared by reading the Readout register. An Attention Request is generated on the bus, only if it is enabled by the Attention Enable bit (ATE) in the Control register.

**Setup Before Enabling** No setup is required for the Voltage-Only Measurement function before it is enabled.

#### 2.10.2 Voltage Capabilities (Addr: 010 000; 10h)

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 010 000 | Voltage Capabilities | R | 0051h | Reserved | | | | | | | # of Voltage Sensors | | | | | Rout Size | 9-bit Resolution | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |

This register defines the format of the voltage data in the voltage readout register. The LM41 only supports one format for all voltage measurements as defined by the values of this register.

| Bit | Type | Description |
|---|---|---|
| 2-0 | RO | **Resolution.** This field defines the total number of significant bits in the Voltage Readout field in the Readout register for this function. The voltage data is always aligned to the left in the Voltage Readout filed and is extended with zeros.<br>001: 9-bit (value for the LM41 for other field values see the SensorPath specification) |
| 3 | RO | **RoutSize (Readout Register size).** Defines the total size of the Readout register.<br>0: 16 bits. (value for the LM41 for other field values see the SensorPath specification) |
| 8-4 | RO | **# of Voltage Sensors (Number of Voltage Sensors).** Specifies the number of Voltage Sensors supported by this function.<br>5: The number of Voltage Sensors. (value for the LM41 for other field values see the SensorPath specification) |
| 15-9 | RO | **Reserved.** Will always read "0". |

#### 2.10.3 Voltage Readout (Addr: 010 001; 11h)

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 010 001 | Voltage Readout | R | | Voltage Readout | | | | | | | | | Reserved | | SNUM | | | Reserved | |
| | | | | MSb | | | | | | | | LSb | 0 | 0 | | | | 0 | 0 |

| Bit | Type | Description |
|---|---|---|
| 0-1 | RO | **Reserved.** Will always read "0". |
| 4-2 | RO | **SNUM (Sensor Number).** This field indicates the number of the current Voltage Sensor, to which the data in the Voltage Readout field belongs. See *Table Analog Input Voltage Mapping* for assignments. |
| 6-5 | RO | **Reserved.** Will always read "0". |
| 15-7 | RO | **Voltage Readout.** This field holds the result of the voltage measurement. The active size of this field for the LM41 is 9-bits, left justified. See *Table Analog Input Voltage Mapping* for voltage mapping details. |

## 2.0 Register Set (Continued)

**Analog Input Voltage Mapping**

| Sensor Number (SNUM) | Voltage Input | Input Voltage for Nominal Reading (code 384 or 180h) | Maximum Input Voltage Range (V for code 510.5 to Max $V_{IN}$ for pin) | Register Reading at Maximum Voltage Range | Minimum Input Voltage | Register Reading at Minimum Voltage | Resolution |
|---|---|---|---|---|---|---|---|
| 0 | +2.5V | 2.5V | 3.32V to 6V | 1FFh | -0.5V to 3.26mV | 00h | 6.51mV |
| 1 | +1.2V | 1.2V | 1.6V to 6V | 1FFh | -0.5V to 2.63mV | 00h | 5.86mV |
| 2 | +3.3V_SBY (V+) | 3.3V | 4.39V to 6V | 1FFh | 3.0V | 15Dh | 8.59mV |
| 3 | +5V | 5V | 6.65V | 1FFh | -0.5V to 6.51mV | 00h | 13.02mV |
| 4 | +12V | 12V | 15.95V to 16V | 1FFh | -0.5V to 15.63mV | 00h | 31.25mV |

### 2.10.4 Voltage Control (Addr: 010 010; 12h)

This register is set to the reset value by a Device Reset.

| Reg Add | Register Name | R/W | POR Val | Bit 15 MSb | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 010 010 | Voltage Control | R/W | 1Fh | Reserved | | | | | EN4 | EN3 | EN2 | EN1 | EN0 | ATE | Low Rate Function (Read Only) | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | | | | | | | 1 | 1 | 1 | 1 | 1 |

| Bit | Type | Description |
|---|---|---|
| 4-0 | RO | **Low Rate Function** This function is not supported by the LM41 and therefore this field is read only. |
| 5 | R/W | **ATE (Attention Enable).** When set, this bit enables an Attention Request signal to be generated by the LM41, if one or more EN0-EN4 bits of this register are set.<br>0: Attention Request disabled (from enabled Temperature Sensor- default)<br>1: Attention Request enabled |
| 6 | R/W | **EN0 (Enable Sensor 0).** When this bit is set, the Voltage Sensor 0 is enabled for voltage measurements.<br>0: Voltage Sensor disabled (default)<br>1: Voltage Sensor enabled |
| 10-7 | R/W | **EN1-EN4 (Enable Sensor 1-4).** Same as EN0 for Voltage sensors 1-4.<br>0: Voltage Sensor disabled (default)<br>1: Voltage Sensor enabled |
| 15-11 | RO | **Reserved.** Will always read "0". |

### 2.11 CONVERSION RATE (Addr: 100 000; 20h)

| Reg Add | Register Name | R/W | POR Val | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 LSb |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 000 | Conversion Rate | R/W | 2h | Reserved | | | | | | CR1 | CR0 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | | |

## 2.0 Register Set (Continued)

| Bit | Type | Description |
|---|---|---|
| 1-0 | RO | **CR0 and CR1 (Conversion Rate bits 0 and 1)** These bits control the conversion rate of the LM41 for more details see *Table Conversion Rate Control* and desciption below. |
| 7-2 | RO | **Reserved.** Will always read "0". |

**Conversion Rate Control**

| LowPwr | [CR1:CR0] | Typical Conversion Rate (ms) |
|---|---|---|
| 0 | 00 | Fastest*: continuous |
| 1 | 00 | 91 |
| 0 | 01 | 91 |
| 1 | 01 | 364 |
| 0 | 10 | 182 (default) |
| 1 | 10 | 728 |
| 0 | 11 | 364 |
| 1 | 11 | 1456 |

*Fastest: 7.5ms(remote) + 7.5msec (local) + 5x1.42msec (voltage) = 22.1 ms total

The sensor conversion rate is controlled by this register as well as the Low Power Bit of Device Control Register. This register is not defined by the SensorPath specification. Therefore, when using a Super I/O host on a motherboard this register must be modified during BIOS run time. The conversion rate is dependent on system physical requirements and limitations. The thermal response time of the MSOP package is one such requirement. Most systems will function properly with the default settings. The master scan rate is related to the conversion rate of the LM41. If attentions are enabled the conversion rate and scan rate will be equal.

## 3.0 Application Hints

The LM41 can be applied easily in the same way as other integrated-circuit temperature sensors, and its remote diode sensing capability allows it to be used in new ways as well. It can be soldered to a printed circuit board, and because the path of best thermal conductivity is between the die and the pins, its temperature will effectively be that of the printed circuit board lands and traces soldered to the LM41's pins. This presumes that the ambient air temperature is almost the same as the surface temperature of the printed circuit board; if the air temperature is much higher or lower than the surface temperature, the actual temperature of the of the LM41 die will be at an intermediate temperature between the surface and air temperatures. Again, the primary thermal conduction path is through the leads, so the circuit board temperature will contribute to the die temperature much more strongly than will the air temperature.

To measure temperature external to the LM41's die, use a remote diode. This diode can be located on the die of a target IC, allowing measurement of the IC's temperature, independent of the LM41's temperature. The LM41 has been optimized to measure the remote diode of a 90 nm Pentium 4 processor as shown in *Figure 7*. A discrete diode can also be used to sense the temperature of external objects or ambient air. Remember that a discrete diode's temperature will be affected, and often dominated, by the temperature of its leads.

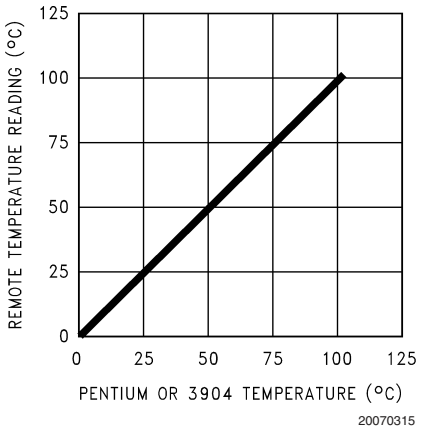



**FIGURE 7. 90 nm Pentium 4 Temperature vs LM41 Temperature Reading**

Most silicon diodes do not lend themselves well to this application. It is recommended that a 2N3904 transistor base emitter junction be used with the collector tied to the base.

A diode connected 2N3904 approximates the junction available on a Pentium microprocessor for temperature measurement. Therefore, the LM41 can sense the temperature of this diode effectively. Although, an offset will be observed. The temperature reading will be offset by approximately –4.5˚C, therefore a correction factor of +4.5˚C should be added to all temperature readings when using a 2N3904 transistor.

# 3.0 Application Hints (Continued)

### 3.1 DIODE NON-IDEALITY

#### 3.1.1 Diode Non-Ideality Factor Effect on Accuracy

When a transistor is connected as a diode, the following relationship holds for variables $V_{BE}$, T and $I_f$:

$$I_F = I_S \left[ e^{\frac{V_{be}}{\eta V_t}} - 1 \right]$$

where:

$$V_t = \frac{k\,T}{q}$$

- q = $1.6 \times 10^{-19}$ Coulombs (the electron charge),
- T = Absolute Temperature in Kelvin
- k = $1.38 \times 10^{-23}$joules/K (Boltzmann's constant),
- $\eta$ is the non-ideality factor of the process the diode is manufactured on,
- $I_S$ = Saturation Current and is process dependent,
- $I_f$= Forward Current through the base emitter junction
- $V_{BE}$ = Base Emitter Voltage drop

In the active region, the -1 term is negligible and may be eliminated, yielding the following equation

$$I_F = I_S \left[ e^{\frac{V_{be}}{\eta V_t}} \right]$$

In the above equation, $\eta$ and $I_S$ are dependant upon the process that was used in the fabrication of the particular diode. By forcing two currents with a very controlled ration (N) and measuring the resulting voltage difference, it is possible to eliminate the $I_S$ term. Solving for the forward voltage difference yields the relationship:

$$V_{be} = \eta \frac{k\,T}{q} \ln (N)$$

The non-ideality factor, $\eta$, is the only other parameter not accounted for and depends on the diode that is used for measurement. Since $\Delta V_{BE}$ is proportional to both $\eta$ and T, the variations in $\eta$ cannot be distinguished from variations in temperature. Since the non-ideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the Pentium III Intel specifies a ±1% variation in $\eta$ from part to part. As an example, assume a temperature sensor has an accuracy specification of ±3˚C at room temperature of 25 ˚C and the process used to manufacture the diode has a non-ideality variation of ±1%. The resulting accuracy of the temperature sensor at room temperature will be:

$$T_{ACC} = \pm 3^{\circ}C + (\pm 1\% \text{ of } 298\ ^{\circ}K) = \pm 6\ ^{\circ}C$$

The additional inaccuracy in the temperature measurement caused by $\eta$, can be eliminated if each temperature sensor is calibrated with the remote diode that it will be paired with. The following table shows the variations in non-ideality for a variety of processors.

| Processor Family | $\eta$, non-ideality | | | Series R |
|---|---|---|---|---|
| | min | typ | max | |
| Pentium II | 1 | 1.0065 | 1.0173 | |
| Pentium III CPUID 67h | 1 | 1.0065 | 1.0125 | |
| Pentium III CPUID 68h/PGA370Socket/Celeron | 1.0057 | 1.008 | 1.0125 | |
| Pentium 4, 423 pin | 0.9933 | 1.0045 | 1.0368 | |
| Pentium 4, 478 pin | 0.9933 | 1.0045 | 1.0368 | |
| Pentium 4 on 0.13 micron process, 2-3.06GHz | 1.0011 | 1.0021 | 1.0030 | 3.64 Ω |
| Pentium 4 on 90 nm process | | 1.011 | | 3.33 Ω |
| Pentium M Processor (Centrino) | 1.00151 | 1.00220 | 1.00289 | 3.06 Ω |
| MMBT3904 | | 1.003 | | |
| AMD Athlon MP model 6 | 1.002 | 1.008 | 1.016 | |

### 3.2 PCB LAYOUT for MINIMIZING NOISE


**FIGURE 8. Ideal Diode Trace Layout**

In a noisy environment, such as a processor mother board, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM41 can cause temperature conversion errors. Keep in mind that the signal level the LM41 is trying to measure is in microvolts. The following guidelines should be followed:

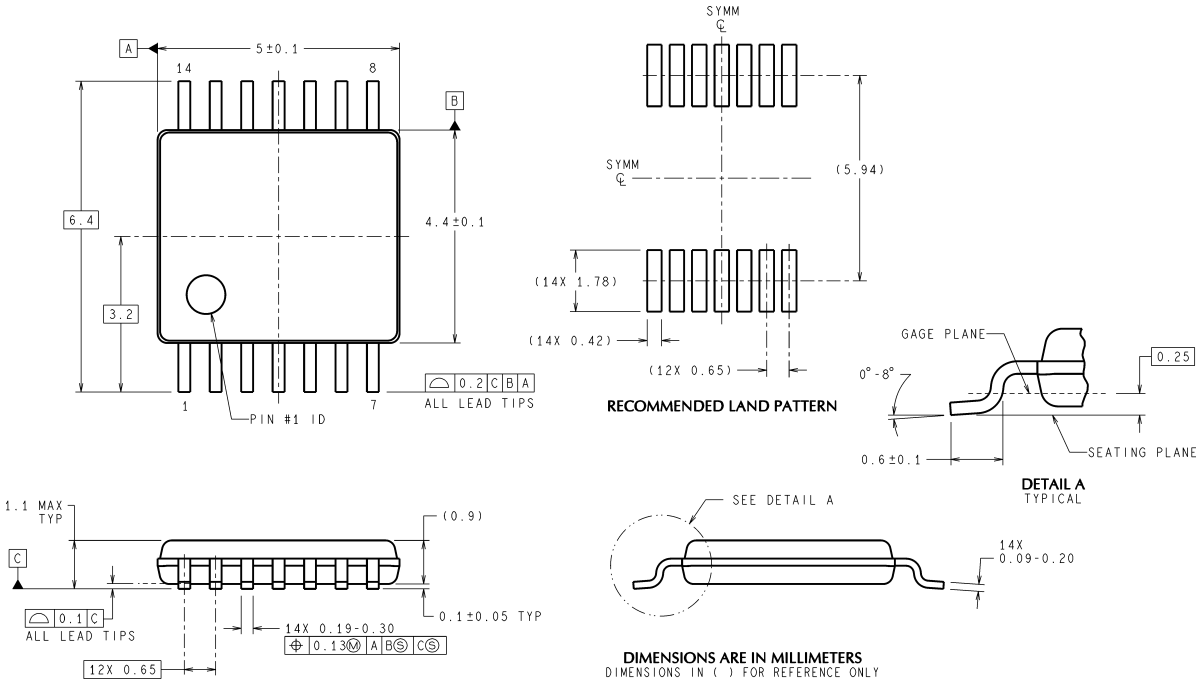
1. Place the 100 pF and 0.1 µF power supply bypass capacitors as close as possible to the LM41's power pin. Place the recommended thermal diode 100 pF capacitor as close as possible to the LM41's D+ and D– pins. Make sure the traces to the thermal diode 100 pF capacitor are matched.
2. The recommended 100 pF diode capacitor actually has a range of 0 pF to 3.3 nF (see curve in Typical Performance Characteristics for effect on accuracy). The average temperature accuracy will not degrade. Increasing the capacitance will lower the corner frequency where differential noise error affects the temperature reading thus producing a reading that is more stable. Conversely, lowering the capacitance will increase the corner frequency where differential noise error affects the temperature reading thus producing a reading that is less stable.

## 3.0 Application Hints (Continued)

3. Ideally, the LM41 should be placed within 10cm of the Processor diode pins with the traces being as straight, short and identical as possible. Trace resistance of 0.7Ω can cause as much as 1˚C of error. This error can be compensated for by adding or subtracting an offset to the remote temperature reading(s).
4. Diode traces should be surrounded by a GND guard ring to either side, above and below if possible. This GND guard should not be between the D+ and D– lines. In the event that noise does couple to the diode lines it would be ideal if it is coupled common mode. That is equally to the D+ and D– lines.
5. Avoid routing diode traces in close proximity to power supply switching or filtering inductors.
6. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2cm apart from the high speed digital traces.
7. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.
8. The ideal place to connect the LM41's GND pin is as close as possible to the Processors GND associated with the sense diode.
9. Leakage current between D+ and GND should be kept to a minimum. Seventeen nano-amperes of leakage can cause as much as 0.2˚C of error in the diode temperature reading (see curve in *Section Typical Performance Characteristics*). Keeping the printed circuit board as clean as possible will minimize leakage current.

The SensorPath Bus is less sensitive to noise than its predecessor the SMBus due to the inherent filtering present in the pulse-width encoding of the data. Care still needs to be taken such that induced noise is analyzed and minimized. SensorPath Bus corrupt data is the most common symptom for noise coupled in SWD. A no-ACK is the symptom for noise coupled into the Device Number Select pin (ADD). An RC lowpass filter as well as a debouncing circuit are included in the LM41 that filter noise spikes less than 2.5 µsec in duration on the SWD signal.

## Physical Dimensions inches (millimeters)
unless otherwise noted




MTC14 (Rev D)

**14-Lead Molded Thin Shrink Small Outline Package (TSSOP,
JEDEC Registration Number MO-153 Variation AB Ref Note 6 dated 7/93,
Order Number LM41CIMT, or LM41CIMTX,
NS Package Number MTC14C**

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